JN3 Hardware User Guide

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Making machines talk.

APPLICABILITY TABLE

PRODUCT
JN3

SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

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Contents

1. Introduction

1.1. Scope

The JN3 is a 12.1mm by 15.9mm integrated GPS receiver module using SiRFstar IV technology. This document expands upon the data sheet(s) to highlight particular areas to allow the hardware engineer to achieve a successful design implementation.

1.2. Audience

This document is intended for helping customer in the integration of the Telit SL868 GPS module

1.3. Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit Technical Support Center (TTSC) at:

http://www.sensorexpert.com.cn 400-883-3391

Alternatively, use:

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

To register for product news and announcements or for product questions contact Telit Technical Support Center (TTSC).

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4. Document Organization

describes the SW updating procedure for Flash

"Chapter 10: "Handling and soldering"

1.5. Text Conventions

or bodily injury may occur.

3. Updating the Firmware: Flash Module (ONLY)

During normal operations, the BOOT signal should be tied to ground through a 100K pulldown resistor. This will ensure the GPS module executes the code out of the internal flash memory.
However, if the internal flash memory needs to be updated, the following steps should be performed to place the JN3 module into a state suitable for programming the internal flash memory.

1. Remove all power to the module.
2. Pull the BOOT signal high through a 10K pull up resistor to +1.8 volts.

   Note: The BOOT signal is not 3.3 volt tolerant.
3. Apply main power.
4. Run the software utility to re-flash the JN3 module. Clearing the entire flash memory is strongly recommended prior to programming.
5. Upon successful completion of re-flashing, remove main power to the module for a minimum of 10 seconds.
6. Pull the BOOT signal low through a 100K pull down resistor to GND.
7. Apply main power to the JN3.
8. Verify the JN3 has returned to the normal operating state.

4. Updating Patch Code: EEPROM and ROM modules with Host Memory

Modules with EEPROM and ROM-only designs using external Host memory support firmware patching. Firmware patches for the EEPROM module are stored inside the I2C serial EEPROM device. Firmware patches for the ROM-only module are stored externally using Host memory.
At power up, patches are retrieved from EEPROM and loaded into patch RAM. Firmware patches are accumulated into patch data files, which in turn are made available with descriptions of their contents and applicability. A patch data file is cumulative in that it includes firmware improvements and enhancements made available in previous patches. It may also include configuration settings that differ from the ROM defaults, as in the default UART baud rate, for example. The desired patch data file must be distributed to the end-user device where it may be accessed by the Host processor.
The Host processor in the end-user device is required to run software that sends patch data from the patch file to the module using OSP Patch Protocol messages over the host serial port. Example source code to assist in the implementation of a patch downloader on the Host processor is available. Note that the module must be operating in full power mode during the patching process. The patch contents are loaded into patch RAM on the module, where they remain as long as main power is maintained. This avoids the reloading of patches into patch RAM when the system resumes normal operation from a low power state such as hibernate. At the end of the patching process the module performs an internal reset and restart.

If main power is lost on the ROM-only module, the Host processor must re-send the patch data over the host serial port after the module is powered up. The Host processor can determine whether patch data must be sent to the module by polling the software version, which reflects the currently applied patch file version.

5. Main Serial Interface

Upon power up, the JN3 will communicate using a standard asynchronous 8 bit protocol (UART) with messages appearing on the TX line, and commands and data being entered on the RX line. There is no parity bit, and no flow control operations are performed.

5.1. Input to the JN3

Maximum sustained inflow at the rate of command messages should not exceed about 10,000 characters per second. Above 115.2kbps, such as 1228800 bps (122880 characters per second), input flow should be limited to less than 10,000 characters/sec to keep from choking the system. Command processing is a low priority task within the system.

At higher data rates, TELIT recommends using OSP message/ACK protocol to prevent message loss.

Low data rates impact startup and TTFF values in sending configuration commands and patches to ROM-based devices and when using host storage for JN3 data files.

5.2. Output from the JN3

Users can control selection and rate of delivery of some output messages through OSP or NMEA configuration commands

Debug messages are controlled as a block and cannot be individually selected.

Some event or alarm messages occur spontaneously and cannot be directly controlled.

You must assess the capacity of the communications link between JN3 and the host. You must select OSP or NMEA messages appropriate to the application and well within the maximum capacity of the communications link. In assessing the capacity required, consider the protocol overheads and maximum size of variable payloads.

In power consumption-critical applications, any time spent creating and sending messages causes both the JN3 and the host to consume power. A low data link speed extends the current consumption of both host and JN3.

5.3. TX/RX Electrical

- “1” (mark) is logic high,
- “0” (space) is logic low,
- idle line = logic high,
- Line-break/open line is continuous logic low: (Continuous break is not allowed on RX during operation and not generated on TX during operation.)
- Do not drive the RX line HIGH if no power is applied to the module

6. MEMS Sensor/EEPROM Interface

The DR I2C port is used for connecting to MEMS sensors, such as accelerometer or magnetometer. Pullup resistors of approximately 2.2Kohm to 1.8 volts are required on the SCL2 and SDA2 lines for proper operation.

Only an approved accelerometer (KIONIX part number KXTF9-4100, 3 x 3mm LGA 1.8V 3 axis accelerometer) can be used. The interrupt output of the accelerometer must be connected to GPIO4 of the JN3.

Data for the approved magnetic sensor (Aichi Steel part number AIM304, 3.5 x 4.0mm 3V 3-axis magnetometer) is output in OSP message 72.

LNA gain of 30 dB for a combined total of 25 dB. However, in the system, antenna X will outperform antenna Y by about 10 dB (refer to Section 7.4 for more details on system noise floor).
An antenna with higher gain will generally outperform an antenna with lower gain. Once the signals are above about -130 dBm for a particular satellite, no improvement in performance would be gained. However, for those satellites that are below about -125 dBm, a higher gain antenna would improve the gain and improve the performance of the GPS receiver. In the case of really weak signals, a good antenna could mean the difference between being able to use a particular satellite signal or not.

7.4. System Noise Floor

As mentioned earlier, the JN3 will display a reported C/No of 40 dB-Hz for an input signal level of -130 dBm. The C/No number means the carrier (or signal) is 40 dB greater than the noise floor measured in a one Hz bandwidth. This is a standard method of measuring GPS receiver performance.
Thermal noise is -174 dBm/Hz at around room temperature. From this we can compute a system noise figure of 4 dB for the JN3. This noise figure consists of the loss of the pre-select SAW filter, the noise figure of the LNA as well as implementation losses within the digital signal processing unit.
If a good quality external LNA is used with the JN3, then the noise figure of that LNA (typically better than 1dB) could reduce the overall system noise figure of the JN3 from 4 dB to around 2 dB. Some of the factors in the system noise figure are implementation losses due to quantization and other factors and do not scale with improved front end noise figure.

7.5. Active versus Passive Antenna

If the GPS antenna is placed near the JN3 and the RF traces losses are not excessive (nominally 1 dB), then a passive antenna can be used. This would normally be the lowest cost option and most of the time the simplest to use. However, if the antenna needs to be located away from the JN3 then an active antenna may be required to obtain the best system performance. The active antenna has its own built in low noise amplifier to overcome RF trace or cable losses after the active antenna.
However, an active antenna has a low noise amplifier (LNA) with associated gain and noise figure. In addition, many active antennas have either a pre-select filter, a post-select filter, or both.

7.6. RF Trace Losses

RF Trace losses are difficult to estimate on a PCB without having the appropriate tables or RF simulation software to estimate what the losses would be. A good rule of thumb would be to keep the RF traces as short as possible, make sure they are 50 ohms impedance and don’t contain any sharp bends.

7.7. Implications of the Pre-select SAW Filter

The JN3 module contains a SAW filter used in a pre-select configuration with the built-in LNA, that is, the RF input of the JN3 ties directly into the SAW filter. Any circuit connected to the input of the JN3 would see complex impedance presented by the SAW filter, particularly out of band, rather than the relatively broad and flat return loss presented by the

LNA. Filter devices pass the desired in band signal to the output, resulting in low reflected energy (good return loss), and reject the out of band signal by reflecting it back to the input, resulting in high reflected energy (bad return loss).
If an external amplifier is to be used with the JN3, the overall design should be checked for RF stability to prevent the external amplifier from oscillating. Amplifiers that are unconditionally stable at the output will be fine to use with the JN3.
If an external filter is to be connected directly to the JN3, care needs to be used in making sure neither the external filter nor the internal SAW filter performance is compromised. These components are typically specified to operate into 50 ohms impedance, which is generally true in band, but would not be true out of band. If there is extra gain associated with the external filter, then a 6 dB Pi or T resistive attenuator is suggested to improve the impedance match between the two components.

7.8. External LNA Gain and Noise Figure

The JN3 can be used with an external LNA such as what might be found in an active antenna. Because of the internal LNA, the overall gain (including signal losses past the external LNA) should not exceed 14 dB. Levels higher than that can affect the jamming detection capability of the JN3. If a higher gain LNA is used, either a resistive Pi or T attenuator can be inserted after the LNA to bring the gain down to 14 dB or the JN3 can be switched into a low gain mode by issuing an OSP command to do so.
The external LNA should have a noise figure better than 1 dB. This will give an overall system noise figure of around 2 dB assuming the LNA gain is 14 dB, or if higher the low gain mode is selected within the JN3.
The external LNA, if having no pre-select filter, needs to be able to handle other signals other than the GPS signal. These signals are typically at much higher levels. The amplifier needs to stay in the linear region when presented with these other signals. Again, the system designer needs to determine all of the unintended signals and their possible levels that can be presented and make sure the external LNA will not be driven into compression. If this were to happen, the GPS signal itself would start to be attenuated and the GPS performance would suffer.

7.9. Powering the External LNA (active antenna)

The external LNA needs a source of power. Many of the active antennas accept a 3 volt or 5 volt DC voltage that is impressed upon the RF signal line. This voltage is not supplied by the JN3, but can be easily supplied by the host design.
Two approaches can be used. The first is to use an inductor to tie directly to the RF trace. This inductor should be at self resonance at L1 (1.57542 GHz) and should have good Q for low loss – the higher the Q, the lower the loss. The side of the inductor connecting to the antenna supply voltage should be bypassed to ground with a good quality RF capacitor, again operating at self resonance at the L1 frequency.
The second approach is to use a quarter-wave stub in place of the inductor. The length of the stub is designed to be exactly a quarter-wavelength, which has the effect of making an RF short at L1 at one end of the stub to appear as an RF open. The RF short is created by the good quality RF capacitor operating at self resonance.
The choice between the two would be determined by:

- RF path loss introduced by either the inductor or quarter wave stub.
- Cost of the inductor.
- Space availability for the quarter wave stub.

Simulations done by Telit show the following:

- Murata LQG15HS27NJ02 Inductor 0.65 dB of additional signal loss
- Quarter wave stub on FR4 0.59 dB of additional signal loss
- Coilcraft B09TJLC Inductor (used in ref. design) 0.37 dB of additional signal loss

This additional loss occurs after the LNA in the active antenna, so it is generally not significant unless the circuit is being designed to work with either an active or a passive antenna.

7.10. RF Interference

RF Interference into the GPS receiver tends to be the biggest problem when determining why the system performance is not meeting expectations. As mentioned earlier, the GPS signals are at -130 dBm and lower. If signal higher than this are presented to the receiver it can be overwhelmed. The JN3 can reject up to 8 CW in-band jamming signals, but would still be affected by non-CW signals.
The most common source of interference is digital noise. This is created by the fast rise and fall times and high clock speeds of modern digital circuitry. For example, a popular netbook computer uses an Atom processor clocked at 1.6 GHz. This is only 25 MHz away from the GPS signal, and depending upon temperature of the SAW filter, can be within the passband of the GPS receiver. Because of the nature of the address and data lines, this would be broadband digital noise at a relatively high level.
Such devices are required to adhere to a regulatory standard for emissions such as FCC Part 15 Subpart J Class B or CISPR 22. However, these regulatory emission levels are far higher than the GPS signal.

7.11. Shielding

Shielding the RF circuitry generally is ineffective because the interference is getting into the GPS antenna itself, the most sensitive portion of the RF path. The antenna cannot be shielded because then it can't receive the GPS signals.
There are two solutions, one is to move the antenna away from the source of interference or the second is to shield the digital interference to prevent it from getting to the antenna.

9. Firmware Configuration

The JN3 can be configured by means of firmware in order to fit better into the overall system. This section describes certain aspects of the receiver that can be configured.

9.1. Internal LNA

The JN3 offers two modes of operation, high gain mode and low gain mode, for the internal LNA. The high gain mode is the default mode and provides 16 to 20dB of gain. The low gain mode provides 6 to 10dB of gain.
In general, the high gain mode is intended for use with passive antennas, while the low gain mode is used when there is an external LNA as part of the RF front end (e.g. active antenna). The recommended external LNA gain is 20dB.
A version of JN3 firmware is offered for system designs that require the low LNA gain mode. The gain mode is selected by the firmware when the receiver starts up. The Tracker Config message (OSP MID178, SID2) can also be used to change the LNA mode, but note that the use of this message is not recommended, because an incorrect parameter could render the JN3 inoperable. Contact Telit technical support if this approach is required in your system.

9.2. TricklePower™ Low Power Mode

In addition to full power mode, the JN3 module can be operated in the TricklePower™ power management mode. Full power mode consumes more average power, but it is the more accurate navigation mode and supports the most dynamic motion scenarios. TricklePower mode is a duty-cycling mode. It provides navigation updates at a fixed rate and retains a high quality of GPS accuracy and dynamic motion response, but at a lower average power cost as compared to Full Power operation. TricklePower mode produces significant power savings in strong signal conditions.
Depending upon the requirements of the system design regarding frequency of position updates and availability of GPS signals in the operational environment, the designer can choose the mode that provides the better trade-off of performance versus power consumption. TricklePower mode can be commanded using the Power Mode Request Message (MID218), which is available as part of the OSP message set. This message can also be used to command the receiver back to Full Power mode. More details regarding low power operation can be found in the Low Power Operating Modes Application Note.

10.2. ESD

The JN3 is an electrostatic discharge sensitive device and should be handled in accordance with JESD625-A requirements for Handling Electrostatic Discharge Sensitive (ESDS) Devices. Although the JN3 is a module, the expecting handling of the JN3 during assembly and test is identical to that of a semiconductor device.
Note: JEDEC standards are available for free from the JEDEC website http://www.jedec.org.

10.3. Reflow

The JN3 is compatible with lead free soldering processes as defined in IPC/JEDEC J-STD-020. The reflow profile must not exceed the profile given IPC/JEDEC J-STD-020 Table 5-2, "Classification Reflow Profiles". Although IPC/JEDEC J-STD-020 allows for three reflows, the assembly process for the JN3 uses one of those profiles. Thus the JN3 is limited to two reflows.
Note: JEDEC standards are available for free from the JEDEC website http://www.jedec.org.
When reflowing a dual-sided SMT board, it is important to reflow the side containing the JN3 module last. This prevents heavier components within the JN3 becoming dislodged if the solder reaches liquidus temperature while the module is inverted.

10.4. Assembly Issues

Due to the piezo-electric components within the JN3, the component should be placed close to the end of the assembly process to minimize shock to the module. During board singulation, pay careful attention to unwanted vibrations and resonances introduced into the board assembly by the board router.

11. PCB Layout Details

The PCB footprint on the receiving board should match the JN3 pad design shown below.
The solder mask opening is generally determined by the component geometry of other parts on the board and can be followed here.
Standard industry practice is to use a paste mask stencil opening the same dimensions as the pad design.
All dimensions shown are in mm.

Figure 3 – JN3 Pad Design (TOP View)

12. Safety Recommendations

READ CAREFULLY

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc.
- Where there is risk of explosion such as gasoline stations, oil refineries, etc. It is responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity. We recommend following the instructions of the hardware user guides for a correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conforming to the security and fire prevention regulations. The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.
The system integrator is responsible of the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as of any project or installation issue, because the risk of disturbing the GSM network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force. Every module has to be equipped with a proper antenna with specific characteristics. The antenna has
to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case of this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation.

The European Community provides some Directives for the electronic equipments introduced on the market. All the relevant information's are available on the European Community website:

http://ec.europa.eu/enterprise/sectors/rtte/documents/

The text of the Directive 99/05 regarding telecommunication equipments is available, while the applicable Directives (Low Voltage and EMC) are available at:

http://ec.europa.eu/enterprise/sectors/electrical/